AMENDMENTS TO THE CLAIMS

1. (Original) A data driven processing method, comprising:

providing a first set of instructions and incoming data to a first processing unit, of a data driven processor, to operate upon said incoming data;

configuring a data path for transferring data between a second processing unit of the data driven processor and external memory; and

the first processing unit, in response to recognizing that the first set of instructions will require one of reading from and writing to external memory, provides addressing information to a memory access unit of the processor to enable the transfer of additional data between the external memory and the second processing unit via said data path.

2. (Original) The method of claim 1 wherein the first processing unit recognizes an image processing motion vector in said first set of instructions, and said additional data is to be written to the external memory and includes a macro block generated by the second processing unit based on the motion vector.

3. (Original) The method of claim 1 wherein the data path is configured by an external host controller.

4. (Original) The method of claim 1 further comprising:

the first processing unit providing an indication to the memory access unit of whether the transfer is one of a read and a write.

5. (Currently Amended) A data processor comprising:

a first direct memory access (DMA) unit; and

a plurality of processing units each having a plurality of data ports, the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the DMA unit, the plurality of processing units are essentially identical units each having a plurality of sides, each side having a plurality of unidirectional data ports being an input port and an output port wherein the input port is programmable to route incoming data to any one of the output ports.

wherein one of the processing units has a control port from which it is to send information to the DMA unit about setting up a DMA channel through which one of data to be consumed and result data by one of the processing units is transferred.

6. (Original) The processor of claim 5 further comprising:

memory interface circuitry, wherein the DMA unit is to access external memory via the memory interface circuitry.

7. (Original) The processor of claim 6 wherein the memory interface circuitry is on-chip with the DMA unit, the plurality of processing units, and the host interface.

8. (Original) The processor of claim 6 wherein the memory interface circuitry is designed to interface with external memory that is dynamic random access memory.

9. (Currently Amended) The processor of claim 5 wherein ~~the plurality of processing units are essentially identical units each having a plurality of sides, each side having a plurality of unidirectional data ports being an input port and an output port~~each of the processing units has an input programming element (PE) to read incoming data from any one of its input ports, an output PE to write result data to any one of its output ports, and a core PE to execute instructions independently of a data path that is operating through a pair of the input and output ports of that processing unit.

10. Canceled.

11. (Currently Amended) The processor of claim ~~10~~ 1 wherein each of the plurality of processing units has a plurality of control ports on each side including an input control port and an output control port, and wherein the input control port of a processing unit is programmable to route incoming command information to ~~anyone~~ any one of the output control ports of said processing unit.

12. (Original) The processor of claim 9 further comprising an interface to an external device, and wherein the output ports of one of said processing units are

coupled to the input ports of an adjacent one of said processing units except that some of the output ports of an outlying one of said processing units are coupled to the external device interface.

13. (Currently Amended) The processor of claim ~~9~~ 1 further comprising:

a second DMA unit, wherein there are at least four of said plurality of processing units, the data ports on a north side of first and second ones of said four processing units are coupled to the first DMA unit, the data ports on a south side of third and fourth ones of said four processing units are coupled to the second DMA unit, and the data ports of a south side of the first and second processing units are coupled to the data ports of a north side of the third and fourth processing units.

14. (Original) The processor of claim 13 further comprising an interface to an external device, wherein some of the data ports of east and west sides of the processing units are coupled to the external device interface.

15. (Original) The processor of claim 5 further comprising a central processing unit to read and execute instructions that configure the data ports and the DMA unit to create a data channel from one of the processing units to external memory.

16. (Original) The processor of claim 5 further comprising a host interface unit to receive instructions, from an external host controller, that configure the data ports and the DMA unit to create a data path from one of the processing units to external memory.

17. (Original) A system comprising:

a host controller;

external memory;

a data driven processor having a memory access unit to interface the external memory, a plurality of processing units each having a plurality of data ports, the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the memory access unit, and a host interface unit to receive instructions from the external host controller that configure the data ports and the memory unit to create a data path from one of the processing units through a data channel to the external memory,

wherein one of the processing units has a control port which it uses to write data location information to the memory access unit; and

one of a rechargeable battery and a fuel cell coupled to power the external memory, the host controller, and the data driven processor.

18. (Original) The system of claim 17 wherein the host controller includes an embedded processor and its associated main memory.

19. (Original) The system of claim 17 wherein the coupling of each pair of data ports from adjacent processing units is a point-to-point, unidirectional connection.

20. (Original) The system of claim 19 wherein each of the processing units has a core programming element (PE) that can be programmed to execute instructions that operate on incoming data received via an input data port of that processing unit, an input PE that can read data from any one of a plurality of input data ports of that processing unit, and an output PE that can write data to any one of a plurality of output data ports of that processing unit.

21. (Original) The system of claim 20 wherein the core PE of each processing unit can execute its instructions independently of a data path that is operating through a pair of said input and output data ports of that processing unit.

22. (Original) The system of claim 17 wherein the data location information that is sent through the control port includes information about the size and display location of a block of image data.

23. (Original) A system comprising:

external memory;

a data driven processor having a memory access unit to interface the external memory, a plurality of processing units each having a plurality of data ports, the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the memory access unit, and a central processing unit to receive and execute instructions that configure the data ports and the memory unit to create a data path from one of the processing units through a data channel to the external memory, wherein one of the

processing units has a control port which it uses to write data channel information to the memory access unit; and

one of a rechargeable battery and a fuel cell coupled to power the external memory and the data driven processor.

24. (Currently Amended) The system of claim ~~17~~ 23 wherein each of the processing units has a plurality of control ports that are connected to each other in a mesh arrangement so that the data channel information, including one of a read and write command, address, and memory access unit channel identifier, can originate from any one of the processing units and be routed to the memory access unit via a logical control channel programmed in the mesh arrangement.

25. (Original) The system of claim 23 wherein the coupling of each pair of data ports from adjacent processing units is a point-to-point, unidirectional connection.

26. (Original) The system of claim 23 wherein each of the processing units has a plurality of control ports that are coupled to each other and are programmable to allow data channel information to be sent from any one of the processing units to the memory access unit.

27. (Currently Amended) A data processor comprising:

means for translating higher level read and write commands into lower level memory access commands;

a plurality of means for consuming data;

means for implementing programmable data paths to supply data to and accept data from any one of said plurality of data consumption means;

means for receiving instructions, from other than said plurality of data consumption means, to configure the programmable data path implementation means, the plurality of data consumption means, and the higher level read and write translation means; and

means for implementing a programmable control path through said plurality of data consumption means to transfer higher level read and write commands from one of said plurality of data consumption means to the higher level read and write translation means.

28. (Original) The processor of claim 27 further comprising means for ensuring that said lower level memory accesses meet signal level and timing requirements of external memory.

29. (Original) The processor of claim 27 further comprising means for expanding the data processor.